DELAY MATCHING FOR SIGNAL DISTRIBUTION IN A LOGIC CIRCUIT

ABSTRACT

Techniques for compensating for propagation delay differences between signals distributed within a logic circuit. A delay matching circuit mimics the internal clock-to-Q delay produced by a flop. The delay matching circuit is placed in the propagation path of an original signal, such as a clock signal, to be redistributed. In general, the delay matching circuit may include a propagation gate multiplexer have a particular configuration. The delay matching circuit imposes a delay substantially equal to the clock-to-Q delay experienced by divided versions of the original signal. In this manner, the delay matching circuit ensures that the rising and falling edges of the original signal and the divided signal are in substantial alignment, enabling synchronous operation. Hence, the delay matching circuit is capable of synchronizing the redistributed and divided signals.